

FLASH MEMORY WITH BYTE ERASE

ABSTRACT

[0048] A process and a memory architecture is based on "vertical" pages, and support
5 byte by byte erasure. A byte within a "vertical" page is erased, and then other bytes
within the "vertical" page sharing bit lines with the erased byte, are subjected to a
program verify operation after exposure to the stress caused by the erase process. The
other bytes in the page are re-programmed to recover the data if they fail verify.
Therefore, byte erase is executed without the erase/re-program cycling, and only memory
10 cells within the same vertical page as the erased byte, which suffer stress from the erase
potentials on the shared bit lines sufficient to shift their thresholds out of range, are re-
programmed.